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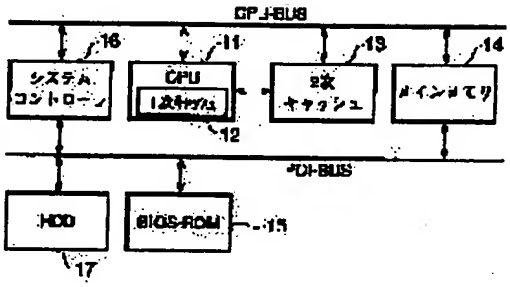
## (54) COMPUTER DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To promote the extension of a battery driving time more by providing a means which performs ON/OFF control over a cache function and incorporating the cache function in a power-saving function.

SOLUTION: A CPU 11 performs a power-saving processing by dynamic effective/ineffective control over a secondary cache according to a power-saving program stored in its main memory 14. Namely, the CPU 11 judges whether or not the secondary cache 13 is already made ineffective in a state below a previously set border value and performs an invalidating processing when the cache is effective. For the invalidating processing for the secondary cache 13 at this time, its contents are written to the main memory 14 as a data saving processing, the secondary cache 13 is then made ineffective, and the supply of an operating clock to the SRAM constituting the secondary cache 13 is stopped to place the SRAM in a sleep state. Consequently, the power consumption of the SRAM constituting the secondary cache 13 is reduced.

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CLAIMS

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[Claim(s)]
[Claim 1] The computer apparatus characterized by having the means which turns on/controls [ off ] a cache function in the computer apparatus equipped with the cache function and the power saving function in which dc-battery actuation is possible, and including a cache function in a power saving function.
[Claim 2] The computer apparatus characterized for a level 2 cache by effective or coming to provide the means changed to an invalid, the means which changes a mode of operation to power-saving mode or normal mode, and the means which confirms a level 2 cache when a mode of operation is normal mode, and makes a level 2 cache an invalid when a mode of operation is in power-saving mode in the computer apparatus equipped with the cache function and the power saving function in which dc-battery actuation is possible.
[Claim 3] The computer apparatus characterized for a level 2 cache by effective or coming to provide the means made into an invalid, a means to acquire the activity ratio of CPU, and a means to cancel a level 2 cache when the activity ratio of CPU is below the set point in the computer apparatus equipped with the cache function in which dc-battery actuation is possible.
[Claim 4] The computer apparatus characterized for a level 2 cache by effective or coming to provide the means made into an invalid, a means to acquire the residual electric energy of a dc-battery, and a means to cancel a level 2 cache when the residual electric energy of a dc-battery is below the set point in the computer apparatus equipped with the cache function in which dc-battery actuation is possible.
[Claim 5] The computer apparatus characterized for a level 2 cache by effective or coming to provide the means made into an invalid, and a means to cancel a level 2 cache at the time of dc-battery actuation in the computer apparatus equipped with the cache function in which dc-battery actuation is possible.
[Claim 6] The computer apparatus according to claim 2, 3, 4, or 5 which performed data evacuation if needed when cancelling a level 2 cache, has the means which carries out reinitialization of the memory content of the cache concerned in case a level 2 cache is validated, and enabled it to perform dynamically the validity / invalid switch of a level 2 cache.

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## DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the computer apparatus equipped with the cache function and the power saving function in which dc-battery actuation is possible. This invention relates to the computer apparatus which made the validity / invalid switch of a cache function one controlled system of a power saving function and in which dc-battery actuation is possible.
[0002]
[Description of the Prior Art] In the small personal computer in which dc-battery actuation is possible, in order to aim at extension of dc-battery actuation time amount, various devices are made. For example, under [, such as residual electric-energy lowering of a user's power-saving mode setting and a dc-battery, ] predetermined conditions, when a key input actuation condition is supervised and there is no key input actuation into the setup time, turn off the back light of a display, or revolution actuation of a hard disk is controlled, or CPU sleep control is performed, and drawing requires reduction-ization of power consumption.
[0003] On the other hand, from the engine-performance side, in order to attain improvement in the speed of memory access, the cache device is adopted. Usually, this seed cache device is comparatively constituted by the cache of small capacity and the comparatively mass cache placed out of the CPU chip placed into the CPU chip. The cache placed out of this CPU chip is called a level 2 cache, an onboard cache, L2 cache, or level 2 cache, and is usually realized on about (256 K bytes or more) several megabytes of SRAM (static RAM).
[0004] By making SRAM which constitutes this level 2 cache sleep under some conditions, lowering of a process speed can be contributed to the cutback of the power consumption of a thing to which are obliged.
[0005] However, in a Prior art, when the reboot of a computer system was needed whenever it switched the validity/invalid of a cache, therefore a user switched the validity/invalid of a cache for the object of engine-performance precedence or dc-battery actuation time amount precedence, application in use, OS, etc. once had to be terminated and there was a problem of being user-unfriendly each time.
[0006] Moreover, in the Prior art, the cache is effective also in the condition of the operating state of a cache being determined regardless of the activity ratio of CPU, therefore not using most CPUs, and the part and power were consumed vainly.
[0007] Moreover, also after the operating state of a cache is determined regardless of the residue (residual electric energy) of a dc-battery, therefore the residue of a dc-battery has decreased, the cache is effective, and a part for power consumption with a useless cache was not able to be made to reflect in extension-ization of dc-battery actuation time amount in a Prior art.
[0008]
[Problem(s) to be Solved by the Invention] By the former, as described above, when the reboot of a computer system was needed whenever it switched the validity/invalid of a cache, therefore a user switched the validity/invalid of a cache for the object of engine-performance precedence or dc-battery actuation time amount precedence, application in use, OS, etc. once had to be terminated and there was a problem of being user-unfriendly each time, in the computer apparatus equipped with the cache function in which dc-battery actuation is possible. Moreover, the cache is effective also in the condition of the operating state of a cache being determined regardless of the activity ratio of CPU, therefore not using most CPUs, and the part and power were

consumed vainly. Furthermore, also after the operating state of a cache is determined regardless of the residue of a dc-battery, therefore the residue of a dc-battery has decreased, the cache is effective, and a part for power consumption with a useless cache was not able to be assigned to extension-ization of dc-battery actuation time amount.

[0009] This invention was made in view of the above-mentioned actual condition, in the computer apparatus equipped with the cache function and the power saving function in which dc-battery actuation is possible, it is putting a cache device on one controlled system of a power saving function, and uses the power consumption accompanying cache actuation for extension-ization of dc-battery actuation time amount, and aims at offering the computer apparatus which can promote extension-ization of dc-battery actuation time amount more by this.

[0010] Moreover, in the computer apparatus equipped with the cache function and the power saving function in which dc-battery actuation is possible, by associating the activity ratio of CPU, and actuation of a cache mutually, this invention reduces the useless power consumption of the cache under the condition which is not using most CPUs, and aims at offering the computer apparatus which can promote a power saving function more.

[0011] Moreover, in the computer apparatus equipped with the cache function and the power saving function in which dc-battery actuation is possible, by associating the residue of a dc-battery, and actuation of a cache mutually, this invention assigns a part for power consumption with a useless cache to extension-ization of dc-battery actuation time amount, and aims at offering the computer apparatus which can promote a power saving function more.

[0012]

[Means for Solving the Problem] This invention is characterized by promoting power-saving more by including a cache device in some controlled systems of a power saving function in the computer apparatus equipped with the cache function and the power saving function in which dc-battery actuation is possible.

[0013] Moreover, this invention is utilizing for a power saving function the means which switches the validity/invalid of a cache dynamically during system behavior, and is characterized by promoting power-saving more.

[0014] That is, in the computer apparatus equipped with the cache function and the power saving function in which dc-battery actuation is possible, this invention has the means which turns on/controls [ off ] a cache function, and is characterized by including a cache function in a power saving function.

[0015] Moreover, this invention is characterized for a level 2 cache by effective or coming to provide the means changed to an invalid, the means which changes a mode of operation to power-saving mode or normal mode, and the means which makes a level 2 cache an invalid when a level 2 cache is confirmed when a mode of operation is normal mode, and a mode of operation is in power-saving mode in the computer apparatus equipped with the cache function and the power saving function in which dc-battery actuation is possible.

[0016] Moreover, this invention is characterized for a level 2 cache by effective or coming to provide the means made into an invalid, a means to acquire the activity ratio of CPU, and a means to cancel a level 2 cache when the activity ratio of CPU is below the set point in the computer apparatus equipped with the cache function in which dc-battery actuation is possible.

[0017] Moreover, this invention is characterized for a level 2 cache by effective or coming to provide the means made into an invalid, a means to acquire the residual electric energy of a dc-battery, and a means to cancel a level 2 cache when the residual electric energy of a dc-battery is below the set point in the computer apparatus equipped with the cache function in which dc-battery actuation is possible.

[0018] Moreover, this invention is characterized for a level 2 cache by effective or coming to provide the means made into an invalid, and a means to cancel a level 2 cache at the time of dc-battery actuation in the computer apparatus equipped with the cache function in which dc-battery actuation is possible.

[0019] Moreover, this invention is characterized by having performed data evacuation if needed, when cancelling a level 2 cache, having the means which carries out reinitialization of the memory content of the cache concerned, in case a level 2 cache is validated, and enabling it to perform dynamically the validity / invalid switch of a level 2 cache in the above-mentioned computer apparatus.

[0020]

[Embodiment of the Invention] With reference to a drawing, 1 operation gestalt of this invention is explained

below. Drawing 1 is the block diagram showing the configuration of the important section of the computer apparatus concerning this invention, and drawing 2 is the power-saving program of the computer apparatus concerning this invention, OS and BIOS, and drawing showing the logical relation of hardware.

[0021] In drawing 1, 11 is CPU which manages system-wide control, and performs power-saving processing by dynamic validity / invalid control of a level 2 cache as shown in drawing 3 thru/or drawing 6 according to the power-saving program shown in drawing 2 here.

[0022] 12 is the cache formed with CPU11 in the CPU chip, and has called the level 1 cache here. SRAM of small capacity constitutes this level 1 cache 12 -- having -- a part of level 2 cache 13 -- data are memorized.

[0023] 13 is a level 2 cache which is set as the object of power-saving processing and which consisted of SRAM, and validity / invalid control is carried out with the system controller 16 later mentioned under control of CPU11 which follows a power-saving program here. The clock of operation supplied to SRAM which constitutes a level 2 cache 13 from control of the system controller 16 which specifically follows processing of the power-saving program of CPU11 is suspended, and it cancels by making a level 2 cache 13 into sleeping. Validation processing is shown for the nullification processing in this case to drawing 3 by the flow chart again at drawing 4 , respectively.

[0024] 14 is main memory (primary storage) with which the processing program storing field of CPU11, a working area, etc. are presented and which was constituted by DRAM (dynamic RAM), and the power-saving program shown in drawing 2 here and OS, a driver, etc. are stored.

[0025] 15 is BIOS-ROM which stored the control program which CPU11 performs. 16 is a system controller which performs system control to the bottom of control of CPU11, suspends the clock of operation supplied at SRAM which constitutes a level 2 cache 13 to the bottom of control of CPU11 which follows a power-saving program here, and cancels a level 2 cache 13 by making a level 2 cache 13 into sleeping. The nullification processing in this case is shown in drawing 3 , and validation processing is shown in drawing 4 , respectively.

[0026] Above-mentioned CPU11, a level 2 cache 13 and main memory 14, and a system controller 16 are mutually connected through a CPU bus (CPU-BUS), respectively.

[0027] Moreover, 15 and 17 are the storage connected to the PCI bus (PCI-BUS), respectively, and BIOS-ROM in which 15 stored the control program of CPU11, and 17 are the hard disk drives (HDD) used as enternal memory.

[0028] In addition, although the power source for actuation of the above-mentioned component is supplied by the dc-battery power source which used the AC power or the rechargeable battery, it omits and shows the power circuit here. Drawing 3 and drawing 4 are flow charts which show the procedure at the time of carrying out validity / invalid control of the level 2 cache 13, respectively, among these drawing 3 shows the procedure at the time of cancelling a level 2 cache 13, and drawing 4 shows the procedure at the time of validating a level 2 cache 13.

[0029] Drawing 5 and drawing 6 are flow charts which show the procedure at the time of carrying out validity / invalid control of the level 2 cache 13 dynamically as an object of an power saving force control using the validity / invalid control function of a level 2 cache 13 shown in above-mentioned drawing 3 and drawing 4 , respectively, among these drawing 5 shows the procedure at the time of carrying out validity / invalid control of the level 2 cache 13 according to the activity ratio of CPU11, and drawing 6 shows the procedure at the time of carrying out validity / invalid control of the level 2 cache 13 according to a dc-battery residue.

[0030] Here explains the actuation in the operation gestalt of this invention with reference to each above-mentioned drawing. CPU11 performs power-saving processing by dynamic validity / invalid control of a level 2 cache as shown in drawing 3 thru/or drawing 6 according to the power-saving program stored in main memory 14.

[0031] First, with reference to drawing 1 thru/or drawing 5 , the processing actuation at the time of carrying out validity / invalid control of the level 2 cache 13 according to the activity ratio of CPU11 is explained. Progress of the activity ratio polling time amount of CPU11 acquires a CPU activity ratio ( drawing 5 steps S51 and S52). (or calculation)

[0032] Here, when it judges whether the level 2 cache 13 is already an invalid when it is in the condition that CPU11 is lower than the boundary value set up beforehand ( drawing 5 step S53) ( drawing 5 step S54) and is in an effective condition, nullification processing shown in drawing 3 is performed ( drawing 5 step S56). In

addition, in the nullification processing shown in this drawing 3 , the example at the time of taking adjustment of memory data with a write back (store-in) method is shown, and it becomes unnecessary processing [ of step S31 in drawing ] in the case of a write-through (store-through) method.

[0033] After it writes out the content of the level 2 cache 13 on main memory 14 and performs data evacuation, nullification processing of the level 2 cache 13 in this case makes a level 2 cache 13 an invalid, suspends supply of the clock of operation to SRAM which constitutes a level 2 cache 13, and makes SRAM sleeping ( drawing 3 steps S31-S33). The power consumption of SRAM which constitutes a level 2 cache 13 by this is reduced.

[0034] Moreover, in decision ( drawing 5 step S54) whether the level 2 cache 13 is already an invalid, when the level 2 cache 13 is already an invalid, processing is ended.

[0035] Moreover, in decision ( drawing 5 step S53) whether it is in the condition that CPU11 is lower than the boundary value set up beforehand, when a level 2 cache 13 judges whether it is already effective when it is beyond the boundary value to which CPU11 was set beforehand ( drawing 5 step S55), and it is in an invalid state, validation processing shown in drawing 4 is performed ( drawing 5 step S57).

[0036] After validation processing of the level 2 cache 13 in this case resumes supply of the clock of operation to SRAM which constitutes a level 2 cache 13 and makes the SRAM concerned an active state, it initializes a level 2 cache 13 and confirms a level 2 cache 13 ( drawing 4 steps S41-S43).

[0037] Moreover, in decision ( drawing 5 step S55) whether the level 2 cache 13 is already effective, when the level 2 cache 13 is already effective, processing is ended.

[0038] Next, with reference to drawing 1 thru/or drawing 4 , and drawing 6 , the processing actuation at the time of carrying out validity / invalid control of the level 2 cache 13 according to a dc-battery residue (residual electric energy) is explained. If a dc-battery residue changes at the time of dc-battery actuation, the change will be notified to CPU11.

[0039] It judges whether CPU11 became lower than the boundary value to which the notified dc-battery residue was set beforehand, when advice of a dc-battery residue is received ( drawing 6 steps S61 and S62).

[0040] Here, when it judges whether the level 2 cache 13 is already an invalid when a dc-battery residue is below the boundary value set up beforehand ( drawing 6 step S63) and is in an effective condition, nullification processing shown in drawing 3 is performed ( drawing 6 step S64).

[0041] Nullification processing of the level 2 cache 13 in this case is as having mentioned above, and omits that explanation of operation here. Moreover, in decision ( drawing 6 step S64) whether the level 2 cache 13 is already an invalid, when the level 2 cache 13 is already an invalid, processing is ended.

[0042] Moreover, in decision ( drawing 6 step S62) whether it is below the boundary value to which the dc-battery residue was set beforehand, when a level 2 cache 13 judges whether it is already effective when it is beyond the boundary value to which the dc-battery residue was set ( drawing 6 step S64), and it is in an invalid state, validation processing shown in drawing 4 is performed ( drawing 6 step S66).

[0043] Validation processing of the level 2 cache 13 in this case is as having mentioned above, and omits that explanation of operation here. Moreover, in decision ( drawing 6 step S64) whether the level 2 cache 13 is already effective, when the level 2 cache 13 is already effective, processing is ended.

[0044] As described above, according to the operation gestalt of this invention, by putting a cache device on one controlled system of a power saving function, the power consumption accompanying cache actuation is used for extension-ization of dc-battery actuation time amount, and, thereby, extension-ization of dc-battery actuation time amount can be promoted more. Moreover, by associating the activity ratio of CPU, and actuation of a cache mutually, the useless power consumption of the cache under the condition which is not using most CPUs is reduced, and a power saving function can be promoted more. Furthermore, by associating the residue of a dc-battery, and actuation of a cache mutually, a part for power consumption with a useless cache is assigned to extension-ization of dc-battery actuation time amount, and a power saving function can be promoted more.

[0045] In addition, although the validity / invalid switch of cache memory were performed by the power-saving program with the above-mentioned operation gestalt, it is also possible to carry out execution control by other drivers (software) which operate on OS, or BIOS (firmware).

[0046]

[Effect of the Invention] As a full account was given above, the power consumption accompanying cache

actuation is used for extension-ization of dc-battery actuation time amount by putting a cache device on one controlled system of a power saving function in the computer apparatus which was equipped with the cache function and the power saving function according to this invention and in which dc-battery actuation is possible, and the computer apparatus which can promote extension-ization of dc-battery actuation time amount more by this can be offered.

[0047] Moreover, in the computer apparatus equipped with the cache function and the power saving function in which dc-battery actuation is possible, by associating the activity ratio of CPU, and actuation of a cache mutually, the useless power consumption of the cache under the condition which is not using most CPUs is reduced, and, according to this invention, the computer apparatus which can promote a power saving function more can be offered.

[0048] Moreover, in the computer apparatus equipped with the cache function and the power saving function in which dc-battery actuation is possible, by associating the residue of a dc-battery, and actuation of a cache mutually, a part for power consumption with a useless cache is assigned to extension-ization of dc-battery actuation time amount, and, according to this invention, the computer apparatus which can promote a power saving function more can be offered.

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## TECHNICAL FIELD

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[Field of the Invention] This invention relates to the computer apparatus equipped with the cache function and the power saving function in which a dc-battery drive is possible. This invention relates to the computer apparatus which made effective / invalid switch of a cache function one controlled system of a power saving function and in which a dc-battery drive is possible.

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PRIOR ART

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[Description of the Prior Art] In the small personal computer in which a dc-battery drive is possible, in order to aim at extension of dc-battery drive time amount, various devices are made. For example, under [, such as a residual electric-energy fall of a user's power-saving mode setting and a dc-battery, ] predetermined conditions, when a key input actuation condition is supervised and there is no key input actuation into the setup time, turn off the back light of a display, or the rotation drive of a hard disk is controlled, or CPU sleep control is performed, and reduction-ization of power consumption is attained.

[0003] On the other hand, from the engine-performance side, in order to attain improvement in the speed of memory access, the cache device is adopted. Usually, this seed cache device is comparatively constituted by the cache of small capacity and the comparatively mass cache placed out of the CPU chip placed into the CPU chip. The cache placed out of this CPU chip is called a level 2 cache, an onboard cache, L2 cache, or level 2 cache, and is usually realized on about (256 K bytes or more) several megabytes of SRAM (static RAM).

[0004] By making SRAM which constitutes this level 2 cache sleep under some conditions, the fall of a process speed can be contributed to reduction of the power consumption of that to which are obliged.

[0005] However, in a Prior art, when the reboot of a computer system was needed whenever it switched effective/invalid of a cache, therefore a user switched effective/invalid of a cache for the purpose of engine-performance priority or dc-battery drive time amount priority, application in use, OS, etc. once had to be terminated and there was a problem of being user-unfriendly each time.

[0006] Moreover, in the Prior art, the cache is effective also in the condition of the operating state of a cache being determined regardless of the activity ratio of CPU, therefore not using most CPUs, and the part and power were consumed vainly.

[0007] Moreover, also after the operating state of a cache is determined regardless of the residue (residual electric energy) of a dc-battery, therefore the residue of a dc-battery has decreased, the cache is effective, and a part for power consumption with a useless cache was not able to be made to reflect in extension-ization of dc-battery drive time amount in a Prior art.

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EFFECT OF THE INVENTION

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[Effect of the Invention] As a full account was given above, the power consumption accompanying cache actuation is used for extension-ization of dc-battery drive time amount by putting a cache device on one controlled system of a power saving function in the computer apparatus which was equipped with the cache function and the power saving function according to this invention and in which a dc-battery drive is possible, and the computer apparatus which can promote extension-ization of dc-battery drive time amount more by this can be offered.
[0047] Moreover, in the computer apparatus equipped with the cache function and the power saving function in which a dc-battery drive is possible, by associating the activity ratio of CPU, and actuation of a cache mutually, the useless power consumption of the cache under the condition which is not using most CPUs is reduced, and, according to this invention, the computer apparatus which can promote a power saving function more can be offered.
[0048] Moreover, in the computer apparatus equipped with the cache function and the power saving function in which a dc-battery drive is possible, by associating the residue of a dc-battery, and actuation of a cache mutually, a part for power consumption with a useless cache is assigned to extension-ization of dc-battery drive time amount, and, according to this invention, the computer apparatus which can promote a power saving function more can be offered.

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TECHNICAL PROBLEM

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[Problem(s) to be Solved by the Invention] By the former, as described above, when the reboot of a computer system was needed whenever it switched effective/invalid of a cache, therefore a user switched effective/invalid of a cache for the purpose of engine-performance priority or dc-battery drive time amount priority, application in use, OS, etc. once had to be terminated and there was a problem of being user-unfriendly each time, in the computer apparatus equipped with the cache function in which a dc-battery drive is possible. Moreover, the cache is effective also in the condition of the operating state of a cache being determined regardless of the activity ratio of CPU, therefore not using most CPUs, and the part and power were consumed vainly. Furthermore, also after the operating state of a cache is determined regardless of the residue of a dc-battery, therefore the residue of a dc-battery has decreased, the cache is effective, and a part for power consumption with a useless cache was not able to be assigned to extension-ization of dc-battery drive time amount.
[0009] This invention was made in view of the above-mentioned actual condition, in the computer apparatus equipped with the cache function and the power saving function in which a dc-battery drive is possible, it is putting a cache device on one controlled system of a power saving function, and uses the power consumption accompanying cache actuation for extension-ization of dc-battery drive time amount, and aims at offering the computer apparatus which can promote extension-ization of dc-battery drive time amount more by this.
[0010] Moreover, in the computer apparatus equipped with the cache function and the power saving function in which a dc-battery drive is possible, by associating the activity ratio of CPU, and actuation of a cache mutually, this invention reduces the useless power consumption of the cache under the condition which is not using most CPUs, and aims at offering the computer apparatus which can promote a power saving function more.
[0011] Moreover, in the computer apparatus equipped with the cache function and the power saving function in which a dc-battery drive is possible, by associating the residue of a dc-battery, and actuation of a cache mutually, this invention assigns a part for power consumption with a useless cache to extension-ization of dc-battery drive time amount, and aims at offering the computer apparatus which can promote a power saving function more.

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MEANS

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[Means for Solving the Problem] This invention is characterized by promoting power-saving more by including a cache device in some controlled systems of a power saving function in the computer apparatus equipped with the cache function and the power saving function in which a dc-battery drive is possible.
[0013] Moreover, this invention is utilizing for a power saving function the means which switches effective/invalid of a cache dynamically during system behavior, and is characterized by promoting power-saving more.
[0014] That is, in the computer apparatus equipped with the cache function and the power saving function in which a dc-battery drive is possible, this invention has the means which turns on/controls [ off ] a cache function, and is characterized by including a cache function in a power saving function.
[0015] Moreover, this invention is characterized for a level 2 cache by effective or coming to provide the means changed to an invalid, the means which changes a mode of operation to power-saving mode or normal mode, and the means which makes a level 2 cache an invalid when a level 2 cache is confirmed when a mode of operation is normal mode, and a mode of operation is in power-saving mode in the computer apparatus equipped with the cache function and the power saving function in which a dc-battery drive is possible.
[0016] Moreover, this invention is characterized for a level 2 cache by effective or coming to provide the means made into an invalid, a means to acquire the activity ratio of CPU, and a means to cancel a level 2 cache when the activity ratio of CPU is below the set point in the computer apparatus equipped with the cache function in which a dc-battery drive is possible.
[0017] Moreover, this invention is characterized for a level 2 cache by effective or coming to provide the means made into an invalid, a means to acquire the residual electric energy of a dc-battery, and a means to cancel a level 2 cache when the residual electric energy of a dc-battery is below the set point in the computer apparatus equipped with the cache function in which a dc-battery drive is possible.
[0018] Moreover, this invention is characterized for a level 2 cache by effective or coming to provide the means made into an invalid, and a means to cancel a level 2 cache at the time of a dc-battery drive in the computer apparatus equipped with the cache function in which a dc-battery drive is possible.
[0019] Moreover, this invention is characterized by having performed data evacuation if needed, when cancelling a level 2 cache, having the means which carries out reinitialization of the memory content of the cache concerned, in case a level 2 cache is validated, and enabling it to perform dynamically effective / invalid switch of a level 2 cache in the above-mentioned computer apparatus.
[0020]
[Embodiment of the Invention] With reference to a drawing, 1 operation gestalt of this invention is explained below. Drawing 1 is the block diagram showing the configuration of the important section of the computer apparatus concerning this invention, and drawing 2 is the power-saving program of the computer apparatus concerning this invention, OS and BIOS, and drawing showing the logical relation of hardware.
[0021] In drawing 1 , 11 is CPU which manages system-wide control, and performs power-saving processing by dynamic effective / invalid control of a level 2 cache as shown in drawing 3 thru/or drawing 6 according to the power-saving program shown in drawing 2 here.
[0022] 12 is the cache formed with CPU11 in the CPU chip, and has called the level 1 cache here. SRAM of small capacity constitutes this level 1 cache 12 -- having -- a part of level 2 cache 13 -- data are memorized.

[0023] 13 is a level 2 cache which is set as the object of power-saving processing and which consisted of SRAM, and effective / invalid control is carried out with the system controller 16 later mentioned under control of CPU11 which follows a power-saving program here. The clock of operation supplied to SRAM which constitutes a level 2 cache 13 from control of the system controller 16 which specifically follows processing of the power-saving program of CPU11 is suspended, and it cancels by making a level 2 cache 13 into sleeping. Validation processing is shown for the nullification processing in this case to drawing 3 by the flow chart again at drawing 4 , respectively.
[0024] 14 is main memory (primary storage) with which the processing program storing field of CPU11, a working area, etc. are presented and which was constituted by DRAM (dynamic RAM), and the power-saving program shown in drawing 2 here and OS, a driver, etc. are stored.
[0025] 15 is BIOS-ROM which stored the control program which CPU11 performs. 16 is a system controller which performs system control to the bottom of control of CPU11, suspends the clock of operation supplied at SRAM which constitutes a level 2 cache 13 to the bottom of control of CPU11 which follows a power-saving program here, and cancels a level 2 cache 13 by making a level 2 cache 13 into sleeping. The nullification processing in this case is shown in drawing 3 , and validation processing is shown in drawing 4 , respectively.
[0026] Above-mentioned CPU11, a level 2 cache 13 and main memory 14, and a system controller 16 are mutually connected through a CPU bus (CPU-BUS), respectively.
[0027] Moreover, 15 and 17 are the storage connected to the PCI bus (PCI-BUS), respectively, and BIOS-ROM in which 15 stored the control program of CPU11, and 17 are the hard disk drives (HDD) used as enternal memory.
[0028] In addition, although the power source for actuation of the above-mentioned component is supplied by the dc-battery power source which used the AC power or the rechargeable battery, it omits and shows the power circuit here. Drawing 3 and drawing 4 are flow charts which show the procedure at the time of carrying out effective / invalid control of the level 2 cache 13, respectively, among these drawing 3 shows the procedure at the time of cancelling a level 2 cache 13, and drawing 4 shows the procedure at the time of validating a level 2 cache 13.
[0029] Drawing 5 and drawing 6 are flow charts which show the procedure at the time of carrying out effective / invalid control of the level 2 cache 13 dynamically as an object of an power saving force control using effective / invalid control function of a level 2 cache 13 shown in above-mentioned drawing 3 and drawing 4 , respectively, among these drawing 5 shows the procedure at the time of carrying out effective / invalid control of the level 2 cache 13 according to the activity ratio of CPU11, and drawing 6 shows the procedure at the time of carrying out effective / invalid control of the level 2 cache 13 according to a dc-battery residue.
[0030] Here explains the actuation in the operation gestalt of this invention with reference to each above-mentioned drawing. CPU11 performs power-saving processing by dynamic effective / invalid control of a level 2 cache as shown in drawing 3 thru/or drawing 6 according to the power-saving program stored in main memory 14.
[0031] First, with reference to drawing 1 thru/or drawing 5 , the processing actuation at the time of carrying out effective / invalid control of the level 2 cache 13 according to the activity ratio of CPU11 is explained. Progress of the activity ratio polling time amount of CPU11 acquires a CPU activity ratio ( drawing 5 steps S51 and S52). (or calculation)
[0032] Here, when it judges whether the level 2 cache 13 is already an invalid when it is in the condition that CPU11 is lower than the boundary value set up beforehand ( drawing 5 step S53) ( drawing 5 step S54) and is in an effective condition, nullification processing shown in drawing 3 is performed ( drawing 5 step S56). In addition, in the nullification processing shown in this drawing 3 , the example at the time of taking adjustment of memory data with a write back (store-in) method is shown, and it becomes unnecessary processing [ of step S31 in drawing ] in the case of a write-through (store-through) method.
[0033] After it writes out the contents of the level 2 cache 13 on main memory 14 and performs data evacuation, nullification processing of the level 2 cache 13 in this case makes a level 2 cache 13 an invalid, suspends supply of the clock of operation to SRAM which constitutes a level 2 cache 13, and makes SRAM sleeping ( drawing 3 steps S31-S33). The power consumption of SRAM which constitutes a level 2 cache 13 by

this is reduced.

[0034] Moreover, in decision ( drawing 5 step S54) whether the level 2 cache 13 is already an invalid, when the level 2 cache 13 is already an invalid, processing is ended.

[0035] Moreover, in decision ( drawing 5 step S53) whether it is in the condition that CPU11 is lower than the boundary value set up beforehand, when a level 2 cache 13 judges whether it is already effective when it is beyond the boundary value to which CPU11 was set beforehand ( drawing 5 step S55), and it is in an invalid state, validation processing shown in drawing 4 is performed ( drawing 5 step S57).

[0036] After validation processing of the level 2 cache 13 in this case resumes supply of the clock of operation to SRAM which constitutes a level 2 cache 13 and makes the SRAM concerned an active state, it initializes a level 2 cache 13 and confirms a level 2 cache 13 ( drawing 4 steps S41-S43).

[0037] Moreover, in decision ( drawing 5 step S55) whether the level 2 cache 13 is already effective, when the level 2 cache 13 is already effective, processing is ended.

[0038] Next, with reference to drawing 1 thru/or drawing 4 , and drawing 6 , the processing actuation at the time of carrying out effective / invalid control of the level 2 cache 13 according to a dc-battery residue (residual electric energy) is explained. If a dc-battery residue changes at the time of a dc-battery drive, the change will be notified to CPU11.

[0039] It judges whether CPU11 became lower than the boundary value to which the notified dc-battery residue was set beforehand, when the notice of a dc-battery residue is received ( drawing 6 steps S61 and S62).

[0040] Here, when it judges whether the level 2 cache 13 is already an invalid when a dc-battery residue is below the boundary value set up beforehand ( drawing 6 step S63) and is in an effective condition, nullification processing shown in drawing 3 is performed ( drawing 6 step S64).

[0041] Nullification processing of the level 2 cache 13 in this case is as having mentioned above, and omits that explanation of operation here. Moreover, in decision ( drawing 6 step S64) whether the level 2 cache 13 is already an invalid, when the level 2 cache 13 is already an invalid, processing is ended.

[0042] Moreover, in decision ( drawing 6 step S62) whether it is below the boundary value to which the dc-battery residue was set beforehand, when a level 2 cache 13 judges whether it is already effective when it is beyond the boundary value to which the dc-battery residue was set ( drawing 6 step S64), and it is in an invalid state, validation processing shown in drawing 4 is performed ( drawing 6 step S66).

[0043] Validation processing of the level 2 cache 13 in this case is as having mentioned above, and omits that explanation of operation here. Moreover, in decision ( drawing 6 step S64) whether the level 2 cache 13 is already effective, when the level 2 cache 13 is already effective, processing is ended.

[0044] As described above, according to the operation gestalt of this invention, by putting a cache device on one controlled system of a power saving function, the power consumption accompanying cache actuation is used for extension-ization of dc-battery drive time amount, and, thereby, extension-ization of dc-battery drive time amount can be promoted more. Moreover, by associating the activity ratio of CPU, and actuation of a cache mutually, the useless power consumption of the cache under the condition which is not using most CPUs is reduced, and a power saving function can be promoted more. Furthermore, by associating the residue of a dc-battery, and actuation of a cache mutually, a part for power consumption with a useless cache is assigned to extension-ization of dc-battery drive time amount, and a power saving function can be promoted more.

[0045] In addition, although effective / invalid switch of cache memory were performed by the power-saving program with the above-mentioned operation gestalt, it is also possible to carry out execution control by other drivers (software) which operate on OS, or BIOS (firmware).

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[Translation done.]

* NOTICES *



1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.*** shows the word which can not be translated.
3.In the drawings, any words are not translated.

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## DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]
[Drawing 1] The block diagram showing the configuration of the important section of the computer apparatus in the operation gestalt of this invention.
[Drawing 2] The power-saving program of the computer apparatus in the above-mentioned operation gestalt, OS and BIOS, drawing showing the logical relation of hardware.
[Drawing 3] The flow chart which shows the procedure at the time of cancelling the level 2 cache in the above-mentioned operation gestalt.
[Drawing 4] The flow chart which shows the procedure at the time of validating the level 2 cache in the above-mentioned operation gestalt.
[Drawing 5] The flow chart which shows the procedure at the time of carrying out effective / invalid control of the level 2 cache according to the activity ratio of CPU11 in the above-mentioned operation gestalt.
[Drawing 6] The flow chart which shows the procedure at the time of carrying out effective / invalid control of the level 2 cache according to a dc-battery residue in the above-mentioned operation gestalt.
[Description of Notations]
11 -- CPU,
12 -- Cache formed in the CPU chip (level 1 cache),
13 -- Level 2 cache
14 -- Main memory (primary storage),
15 -- BIOS-ROM
16 -- System controller,
17 -- Hard disk drive (HDD).

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[Translation done.]

* NOTICES *



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DRAWINGS

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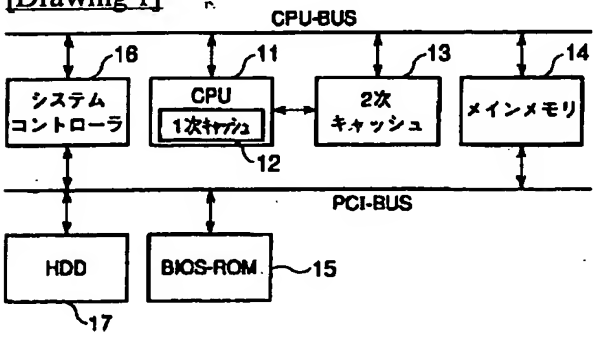
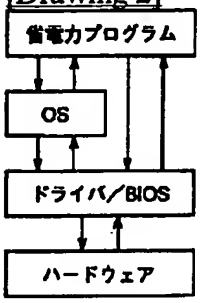
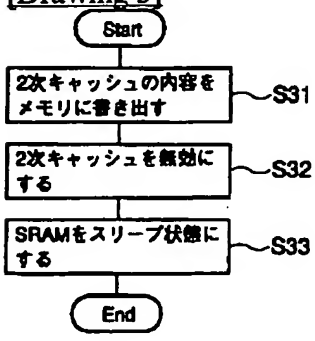
[Drawing 1]



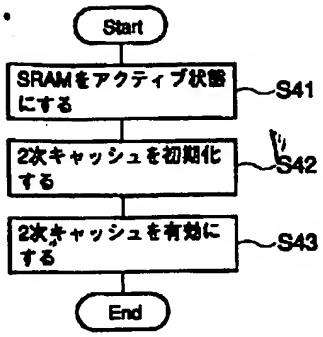

[Drawing 2]



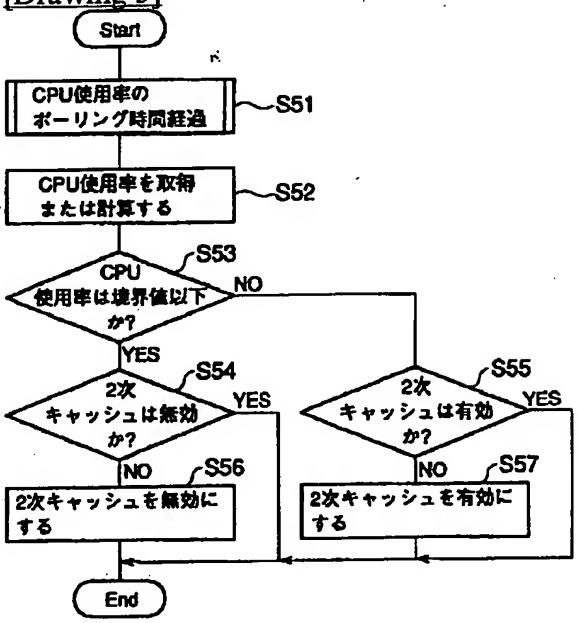

[Drawing 3]



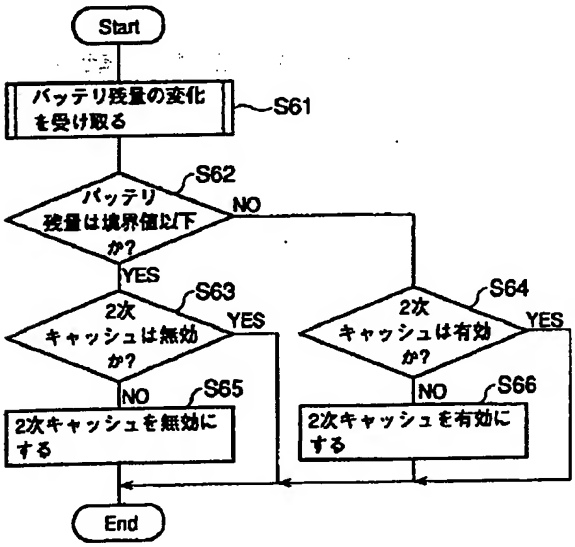

[Drawing 4]




[Drawing 5]




[Drawing 6]

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